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(54) Technique for reducing the number of layers in a multilayer circuit board

(57) A technique for reducing the number of layers in a multilayer circuit board is disclosed. The multilayer circuit board has a plurality of electrically conductive signal layers for routing electrical signals to and from at least one electronic component mounted on a surface of the multilayer circuit board. In one embodiment, the technique is realized by a method for reducing the number of layers in a multilayer circuit board, the multilayer circuit board having a plurality of electrically conductive signal layers for routing electrical signals to and from at least one electronic component mounted on a surface of the multilayer circuit board. The method comprises the steps of: forming a plurality of electrically conductive vias in the multilayer circuit board extending from the surface of the multilayer circuit board to at least one of the plurality of electrically conductive signal layers; arranging the surface such that a first set of two power/ground pins corresponds to first via and a second set of two power/ground pins corresponds to a second via positioned adjacent the first via, thereby creating a channel; and routing a first plurality of electrical signals through the channel on the first of the plurality of electrically conductive signal layers.

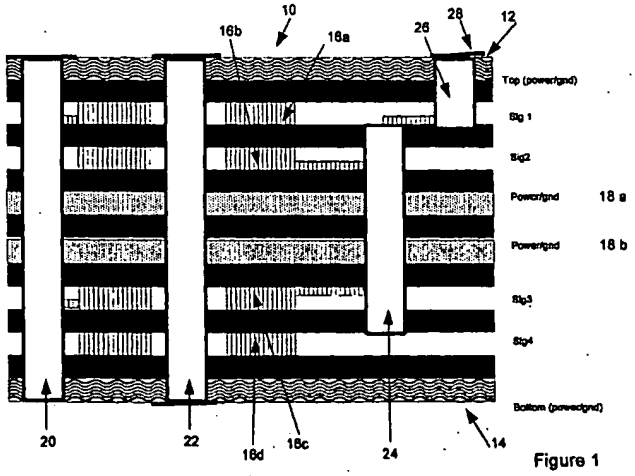

Figure 1

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Description

[0001] The present invention relates generally to multilayer circuit boards and, more particularly, to a technique for reducing the number of layers in a multilayer circuit board.

[0002] The making of electrical connections between electronic components has long been accomplished using printed circuit boards. The first such circuit boards had only a single signal layer on a top surface thereof for routing electrical signals between electronic components mounted thereon. These single signal layer circuit boards have severe limitations with regard to the number of electrical signals that can be routed between electronic components mounted on the same circuit board. That is, the number of electrical signals that can be routed between electronic components mounted on a single signal layer circuit board is limited by the amount of area on the single signal layer.

[0003] The area limitations associated with single signal layer circuit boards led to the development of multilayer printed circuit boards. Such multilayer printed circuit boards may be either single or double-sided and may have multiple signal layers on the surface of and buried within the multilayer printed circuit boards. Thus, such multilayer printed circuit boards have allowed a large increase in the number of electrical signals that may be routed between electronic components mounted on the same circuit board.

[0004] The use of multilayer printed circuit boards has been particularly beneficial when using electronic components having high density packages. That is, electronic components having high density packages generally require multiple layers of a multilayer printed circuit board to make electrical connections with other electronic components mounted on the same circuit board. In fact, the density of electronic component packages typically dictates the number of layers that must be provided by the multilayer printed circuit board upon which the electronic component is mounted. While the number of layers that may be provided by a multilayer printed circuit board is theoretically unlimited, problems occur when the number of layers in a multilayer printed circuit board exceeds a reasonable number, particularly when trying to route high speed electrical signals between electronic components. For example, when making electrical connections between different layers in multilayer printed circuit boards, electrically conductive vias are generally used. While these electrically conductive vias allow direct vertical electrical connections to be made between different layers within a multilayer printed circuit board, there are intrinsic parasitics associated with these electrically conductive vias that can adversely affect the performance of signals propagating therethrough. That is, these electrically conductive vias have intrinsic parasitic resistance, capacitance, and inductance, which can adversely affect signals propagating along each electrically conductive via. In addition, these intrinsic parasitics can also have an adverse effect on the manufacturability of a printed circuit board and thus the cost thereof. Because of their adverse affect on signal performance, these intrinsic parasitics can also limit the bandwidth of signals propagating along each electrically conductive via. These adverse affects only increase as the number of layers in a multilayer printed circuit board increase.

[0005] US Patent No. 6,388,890 published on May 14, 2002 is directed to signal channel routing and also aims to reduce the number of layers in a multilayer circuit board. However, even with the use of the disclosed signal channel routing technique, further improvement is desired.

[0006] In view of the foregoing, it would be desirable to provide a technique for increasing the number of electrical connections that may be made between electronic components mounted on a multilayer printed circuit board without increasing the number of layers in the multilayer printed circuit board. More particularly, it would be desirable to provide a technique for reducing the number of layers in a multilayer circuit board in an efficient and cost effective manner.

[0007] According to the present invention, a technique for reducing the number of layers in a multilayer circuit board is provided. The multilayer circuit board has a plurality of electrically conductive signal layers for routing electrical signals to and from at least one electronic component mounted on a surface of the multilayer circuit board. In a preferred embodiment, the technique is realized by forming a plurality of electrically conductive vias in the multilayer circuit board extending from the surface of the multilayer circuit board to at least one of the plurality of electrically conductive signal layers. The technique is further realized by arranging the surface such that a first set of at least two power/ground pins corresponds to a first via and a second set of at least two power/ground pins corresponds to a second via positioned adjacent the first via, thereby creating a channel on the surface and a channel on a first of the plurality of signal layers, and routing a first plurality of electrical signals through the channel on the first of the plurality of electrically conductive signal layers.

[0008] In accordance with other aspects of the present invention, an improved multilayer circuit board is provided. The multilayer circuit board has a plurality of electrically conductive signal layers for routing electrical signals to and from at least one electronic component mounted on a surface of the multilayer circuit board. The multilayer circuit board comprises a plurality of electrically conductive vias in the multilayer circuit board extending from the surface of the multilayer circuit board to at least one of the plurality of electrically conductive signal layers. The multilayer circuit board additionally comprises a first set of at least two power/ground pins corresponding to a first via and a second set of at least two power/ground pins corresponding to a second via positioned adjacent the first via, arranged to create

a channel on the surface and a channel on a first of the plurality of signal layers,. The multilayer circuit board additionally comprises a first plurality of electrical signal paths routed through the channel on the first of the plurality of electrically conductive signal layers.

[0009] In accordance with further aspects of the present invention, the plurality of electrically conductive signal layers are typically separated by at least one dielectric layer. Also, at least some of the plurality of electrically conductive signal layers are typically separated by at least one electrically conductive power/ground plane layer. Further, the surface of the multilayer circuit board is typically primarily an electrically conductive power/ground plane layer.

[0010] Embodiments of the invention will now be described by way of example with reference to the accompanying drawings, in which:

Figure 1 is a side cross-sectional view of a multilayer printed circuit board in accordance with the present invention.

Figure 2 shows a layout of a surface mount grid array package of an electronic component having 1152 pins.

Figure 3 shows one quadrant (i.e., the upper right quadrant) of the power/ground and signal pins on the top layer of the layout shown in Figure 2.

Figure 4A shows the quadrant of Figure 3 after via placement and pin connection.

Figure 4B shows a cross-sectional view of a multilayer printed circuit board corresponding to the ground (surface) plane layer portion of Figure 4A.

Figure 5A shows a portion of a first signal layer of the multilayer printed circuit board shown in Figure 1.

Figure 5B shows a cross-sectional view of a multilayer printed circuit board corresponding to the signal layer portion of Figure 6A.

Figure 6A shows channel routing of a portion of the first signal layer of the multilayer printed circuit board shown in Figure 1.

Figure 6B shows a cross-sectional view of a multilayer printed circuit board corresponding to the signal layer portion of Figure 4A.

Figure 7A shows a portion of a second signal layer of the multilayer printed circuit board shown in Figure 1.

Figure 7B shows a cross-sectional view of a multilayer printed circuit board corresponding to the second signal layer portion of Figure 7A.

Figure 8 shows a hypothetical 3rd signal layer using conventional thru hole design.

Figure 9 shows all four quadrants of the multilayer board in which the upper right hand corner is a channelized quadrant.

Figure 10 shows doubling up of power pins in order create a free channel on a surface of the multilayer printed circuit board shown in Figure 1.

Figure 11 shows a channelized quadrant of the multilayer printed circuit board of Figure 1; and

Figure 12 shows a standard non-channelized quadrant in contrast to the present invention channelized quadrant of Figure 11.

[0011] A power routing technique of the invention is designed to optimize the free channel routing technique which is disclosed in US Patent No. 6,388,890. As shown in Figure 1, the previously disclosed technique includes a multilayer printed circuit board 10. That is, the multilayer printed circuit board 10 incorporates the concepts of the present invention so as to reduce the number of layers in the multilayer printed circuit board 10.

[0012] The multilayer printed circuit board 10 comprises a primary (top) layer 12, a secondary (bottom) layer 14, a plurality of signal layers 16, and a plurality of power/ground plane layers 18. It should be noted that the primary layer 12 and the secondary layer 14 are primarily power/ground plane layers except for contact pads and test signal runs formed thereon, as will be described in more detail below.

[0013] The multilayer printed circuit board 10 also comprises a first supervia (thru hole) 20 for electrically connecting selected ones of the plurality of signal layers 16 (i.e., signal layers 16a and 16c), a second supervia (thru hole) 22 for electrically connecting the primary layer 12, the secondary layer 14, and selected ones of the plurality of power/ground plane layers 18 (i.e., power/ground plane layers 18a,or 18b,), a buried via 24 for electrically connecting selected ones of the plurality of signal layers 16 (i.e., signal layers 16a and 16d), and a microvia 26 for electrically connecting signal layer 16a to a contact pad 28 formed on the primary layer 12.

[0014] The presently disclosed technique can be used in conjunction with the multilayer printed circuit board 10 shown in Figure 1, or alternatively can be used independently to design clear channels through which additional routing or breakouts can be achieved. Accordingly, the multilayer printed circuit board 10 of Figure 1 is merely exemplary as a conventional multilayer circuit board could readily be employed.

[0015] Referring to Figure 2, there is shown a layout 30 of a surface mount grid array package of an electronic component having 1152 input/output (I/O) contacts. Figure 2 also shows a legend indicating the type of signal associated with I/O contact.

[0016] In order to increase the resolution for purposes of better understanding this detailed description, Figure 3 shows one quadrant 32 (i.e., the upper right quadrant) of the layout 30 shown in Figure 2. Figures 4-7 directly coincide with the quadrant 32 shown in Figure 3. The signal type legend in Figure 2 also applies to Figure 3, as well as to Figures 4B-7B. Figure 4A does not use the legend symbols and is simplified for the sake of clarity. However, Figure 4A shows the same quadrant as shown in Figures 2 and 3 and accordingly has the same layout.

[0017] Referring to Figure 4A, there is shown a portion 34 of the primary layer 12 of the multilayer printed circuit board 10. As indicated above, this portion 34 of the primary layer 12 directly coincides with the quadrant 32 shown in Figure 3. That is, this portion 34 of the primary layer 12 corresponds to the portion of the multilayer printed circuit board 10 where one quadrant of an electronic component having a surface mount grid array package with 1152 I/O contacts is mounted on the multilayer printed circuit board 10.

[0018] As indicated above, the primary layer 12 is primarily a power/ground plane layer except for contact pads and test signal runs formed thereon. More particularly, the primary layer 12 includes a ground plane that is electrically connected to ground contact pads (i.e., GND in legend), but is not electrically connected to power contact pads (i.e., VA and VB in legend), or signal contact pads (i.e., signal in legend).

[0019] As shown in Figure 4A, the power routing technique of the invention strategically utilizes dog bone pads 80 including pins 81 and via 82 arranged in a specific pattern in order to create free channels 90. Note that most dog bone pads 80 used to create the channel include two pins 81. It is also possible to include more than two pins 81 per via 82 with some circuit board designs. All of the pins 81 associated with the via 82 should have the same potential. The doubling of power or ground pin connections 81 on a single via 82 in a specific pattern allows the formation of free channels 90. The doubling of pins 81 per via 82 not only allows formation of channels 90 on the surface of the primary layer 12, but also allows formation of channels in other layers as will be further explained below.

[0020] In many cases, there are just as many (if not more) power and ground pins vs. signal pins in a single package. Therefore it can be seen that using power routing techniques opens up more continuous free channels that can then be used to route signals. Another advantage of the disclosed technique can be seen when routing differential pairs as it allows both signals to be routed side by side vs. being broken up by package pins.

[0021] Figure 4B shows a cross-sectional view of the dog bone pads 80 and component pads 85 mounted on the primary layer 12. Each layer in Figure 4B is corresponds to the layers described above in relation to Figure 1.

[0022] Figure 5A shows a portion 42 of the signal layer 16a of the multilayer printed circuit board 10. As indicated above, this portion 42 of the signal layer 16a directly coincides with the quadrant 32 shown in Figure 3. That is, this portion 42 corresponds to the portion of the multilayer printed circuit board 10 where one quadrant of an electronic component having a surface mount grid array package with 1152 I/O contacts is mounted on the multilayer printed circuit board 10. The signal layer 16a includes channels 72 for accommodating passive components. Unlike with signal channel routing, the power routed channels will actually form on the first signal layer 16a rather than the second signal layer 16b and therefore will provide better distribution of the signals and μvia channels.

[0023] Figure 5B illustrates a cross-sectional view of the signal layer 16A. The choice of via 94 depends upon the selected design. The thru hole via 94 was therefore selected due to the overall stack-up. The use of this thru hole 94 causes channels to be opened on or below the layer 16A.

[0024] Figure 6A further illustrates the upper right quadrant of the signal layer 16A. The signal layer 16a includes a plurality of electrically conductive signal runs 44 that are electrically connected to dog bone vias in the multilayer printed circuit board 10 where channels are formed in other layers of the multilayer printed circuit board 10 in accordance with the present invention. These signal runs 44 are typically preselected based upon the characteristics of the signals they carry. That is, the signals runs 44 may carry high speed signals. Alternatively, the signals runs 44 may carry low speed signals.

[0025] Importantly, as shown in Figure 6B, a μvia 46 that is formed in the multilayer printed circuit board 10 does not extend any further into the multilayer printed circuit board 10 than the signal layer 16a. This allows channels to be formed beneath these μvias 46 in other layers of the multilayer printed circuit board 10, as described in detail below.

[0026] Referring to Figure 7A, there is shown a portion 48 of the signal layer 16b of the multilayer printed circuit board 10. As indicated above, this portion 48 of the signal layer 16b directly coincides with the quadrant 32 shown in Figure 3. That is, this portion 48 of the signal layer 16b corresponds to the portion of the multilayer printed circuit board 10 where one quadrant of an electronic component having a surface mount grid array package with 1152 I/O contacts is mounted on the multilayer printed circuit board 10.

[0027] The signal layer 16b includes a plurality of electrically conductive signal runs 50 that are electrically connected to vias (shown in Figure 7B) formed in the signal layer 16b. In accordance with the present invention, many of these signal runs 50 are routed in the channels 52. That is, the channels formed by the absence of vias in the signal layer 16b in the multilayer printed circuit board 10 allow the plurality of electrically conductive signal runs 50 to be routed therein. Otherwise, if vias were present in these areas 52 in this and other layers of the multilayer printed circuit board 10, then additional signal layers would be required to route the plurality of electrically conductive signal runs 50. Thus, the absence of vias in these areas 52 in this and other layers of the multilayer printed circuit board 10 allow for an overall reduction in the number of signal layers required in the multilayer printed circuit board 10. A massive channel 53 is created where the technique of the US Patent No. 6,388,890 is used in combination with the presently disclosed technique. The massive channel 53

allows routing of additional signals, thereby saving additional space.

[0028] A cross-sectional view of the second signal layer 16b is shown in Figure 7B. A second level μvia 102 can be used in certain situations, particularly if overall layer depth is approximately 9 mil, (the current manufacturing limit). If a via such as the μvia 102 is impracticable due to manufacturing limits, a thru hole 104 can be used. If a μvia is used for power routing, then the main channel formed will be present on all layers below the surface layer 12. Additionally, another channel will be opened on layers below the μvia (i.e. N+1, μvia Top - signal 1 (N=2) will not be visible on or above the third layer since the μvia is so shallow.)

[0029] Figure 8 shows the layer savings afforded by the technique of the invention. In particular, an additional 31 signals would have been required on signal layer three (16c) if conventional thru hole design had been implemented. Accordingly, the technique of the invention (in conjunction with the previously disclosed free channel signal routing) has resulted in a savings of one layer.

[0030] Figure 9 is provided merely to show the comparison between standard quadrants 106 and channelized quadrants 108. As Figure 9 exemplifies, the channelized quadrant results in increased space savings.

[0031] Figure 10 is an additional view of a potential power routing design for a primary layer 12. The free channels 90 result from the positioning of the dog bone pads 80 including pins 81 and via 82. The pins 81 may be power and/or ground pins of the same potential, but do not include signal pins.

[0032] Figure 11 illustrates a channelized quadrant 112 that may appear on any subsequent signal layers that can be combined with signal free channel routing as illustrated in Figure 1 and as described in US Patent No. 6,388,890 such that massive channels can be formed. Signal routing through these massive channels 53 is shown and described above with reference to Figure 7A.

[0033] Figure 12 shows a standard non-channelized quadrant in contrast to the present invention channelized quadrant of Figure 11.

[0034] In summary, the disclosed power routing technique uses strategically placed thru and μvia holes such the free channels can be obtained. Further with the use of μvias, the technique will allow clearance of spaces on subsequent layers within the package footprint which will allow for denser routing within the package.

[0035] This technique focuses on the layer reduction of printed circuit boards. Due to the increase in free channels higher number of signals can be taken out of the package per layer. Further combined with free channel routing the power routing disclosed in US Patent No. 6,388,890, it allows for easier breakouts of high density packages and leads to higher cost savings.

[0036] Previously, although signal pins have been arranged in various patterns, the potential of achieving free channels by the application of power routing has not been explored. The technique of the invention allows free routing channel construction with the use of thru hole vias (or μvias or any other type of blind via depending on the design and board stack-up) and strategic placement of the thru hole (or μvia or blind via) vias with respect to power and ground pins. When combined with signal channel routing, the technique of the invention may be able to provide layer count reduction of 30 - 50%.

[0037] With regard to methodology, the steps used to solve the problem can be summarized as follows: a) Identification of power pins within package footprint; b) Strategic placement of vias such that free channels can be formed; and c) Connection of two or more design permitting pads to one via where ever possible.

[0038] As a further step, d) Power/ground routing can be used to complement signal free channels or vise versa by aligning the two channels together to form a "massive channel".

Claims

1. A method for reducing the number of layers in a multilayer circuit board, the multilayer circuit board having a plurality of electrically conductive signal layers for routing electrical signals to and from at least one electronic component mounted on a surface of the multilayer circuit board, the method comprising the steps of:

   forming a plurality of electrically conductive vias in the multilayer circuit board extending from the surface of the multilayer circuit board to at least one of the plurality of electrically conductive signal layers;
   arranging the surface such that a first set of at least two power/ground pins corresponds to a first via and a second set of at least two power/ground pins corresponds to a second via positioned adjacent the first via, thereby creating a channel on the surface and every layer below which includes a channel on a first of the plurality of signal layers; and
   routing a first plurality of electrical signals through the channel on the first of the plurality of electrically conductive signal layers.

2. The method of claim 1, further comprising the step of forming at least one of the first via and the second via as a thru hole.

3. The method of claim 1, further comprising the step of arranging additional sets of multiple pins with additional vias in order to create a channel of greater length.

4. The method of claim 1, further comprising the step of creating at least one of the first via and the second via as a μvia.

5. The method of claim 1, further comprising the step of creating a channel on a second of the plurality of signal layers.

6. The method of claim 5, further comprising the step of routing a second plurality of electrical signals through the channel on the second of the plurality of signal layers.

7. The method of claim 1, further comprising the step of forming additional electrically conductive vias in the multilayer circuit board extending from the surface of the multilayer circuit board to a first of the plurality of electrically conductive signal layers, the additional electrically conductive vias being arranged so as to form a channel in a second of the plurality of electrically conductive signal layers beneath the first plurality of electrically conductive vias.

8. The method of claim 1, further comprising the step of separating the plurality of electrically conductive signal layers by at least one dielectric layer.

9. The method of claim 1, further comprising the step of arranging via formations in order to create the channels having a preselected width.

10. The method of claim 1, further comprising the step of arranging via formations in order to create a channel of preselected shape including one of: rectangular, square, circular, and diagonal.

11. The method of claim 1, further comprising the step of routing a plurality of electrical signals through channels on plurality of signal layers where the channels are clearly visible.

12. The method of claim 1, further comprising the step of creating an opening in the middle of a chip package through the channel formed by adjacent vias.

13. The method of claim 1, further comprising the step of separating at least some of the plurality of electrically conductive signal layers with at least one electrically conducive power/ground layer.

14. An improved multilayer circuit board, the multilayer circuit board having a plurality of electrically conductive signal layers for routing electrical signals to and from at least one electronic component mounted on a surface of the multilayer circuit board, the multilayer circuit board comprising:

a plurality of electrically conductive vias in the multilayer circuit board extending from the surface of the multilayer circuit board to at least one of the plurality of electrically conductive signal layers;

the surface arranged such that a first set of at least two power/ground pins corresponds to a first via and a second set of at least two power/ground pins corresponds to a second via positioned adjacent the first via, thereby creating a channel on the surface and a channel on a first of the plurality of signal layers; and

a first plurality of electrical signals paths routed through the channel on the first of the plurality of electrically conductive signal layers.

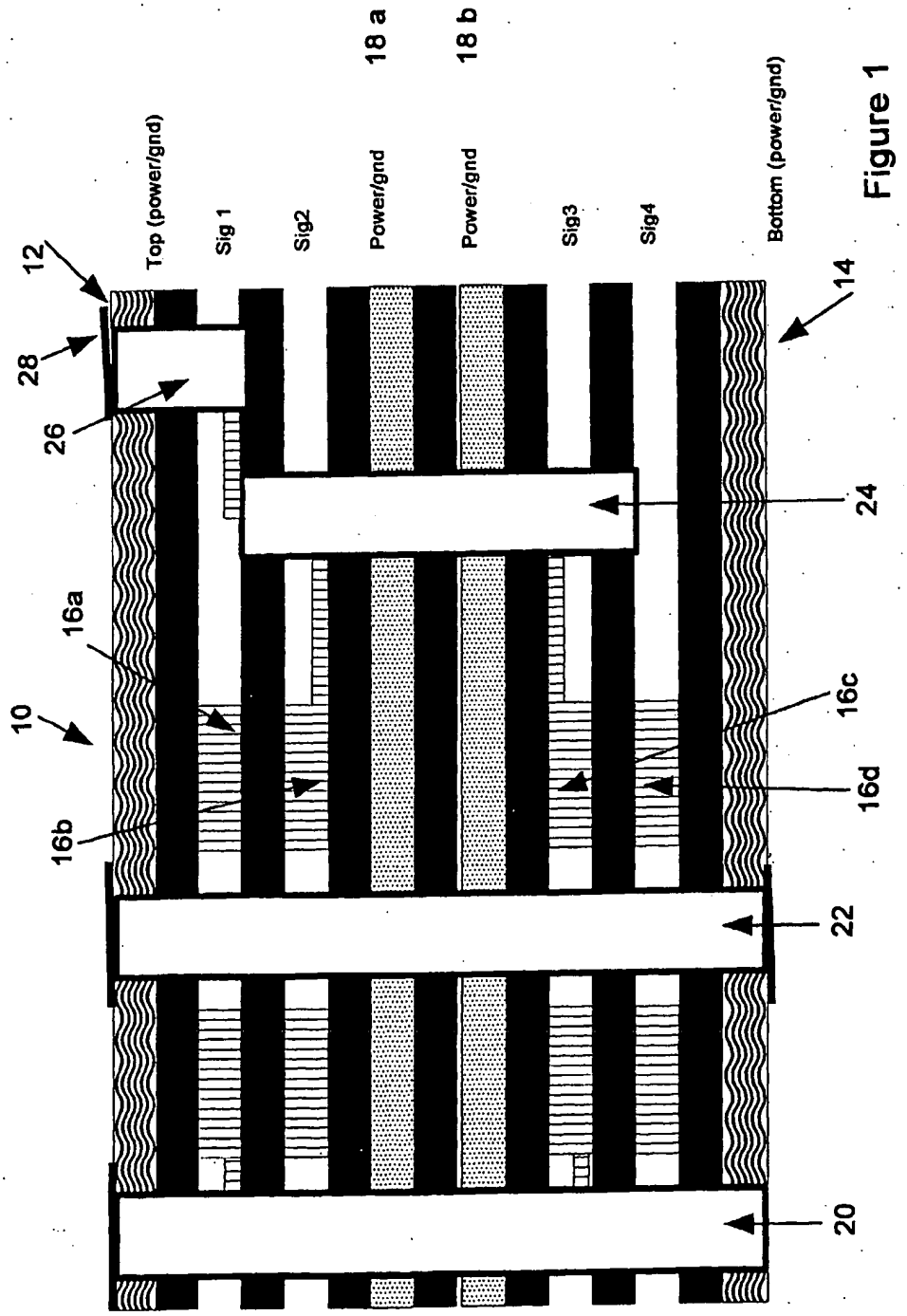

Top (power/gnd)
Sig 1
Sig2
Power/gnd
Power/gnd
Sig3
Sig4
Bottom (power/gnd)
18 a
18 b
12
14
28
26
24
16a
10
16b
16c
16d
22
20

Figure 1

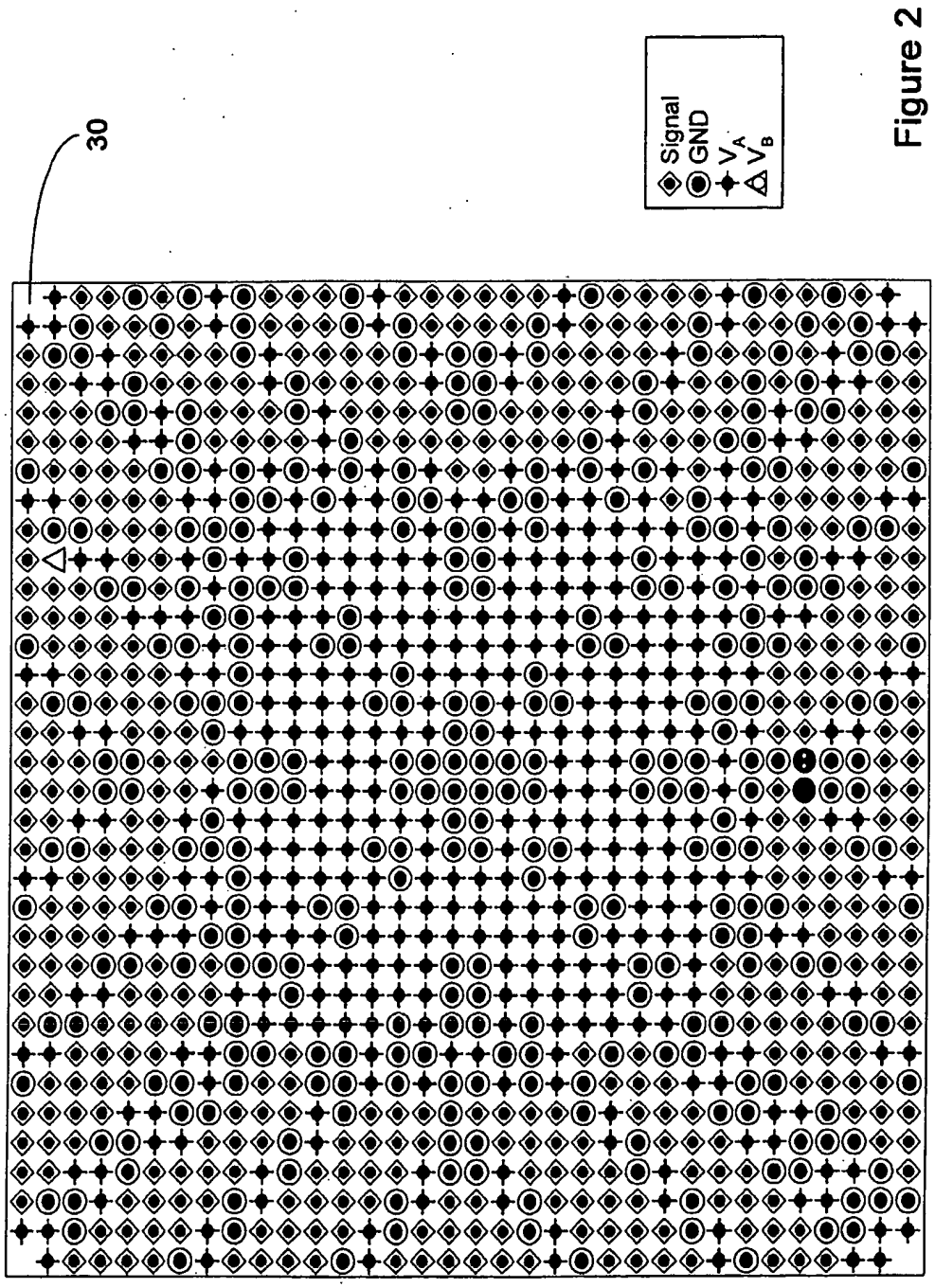
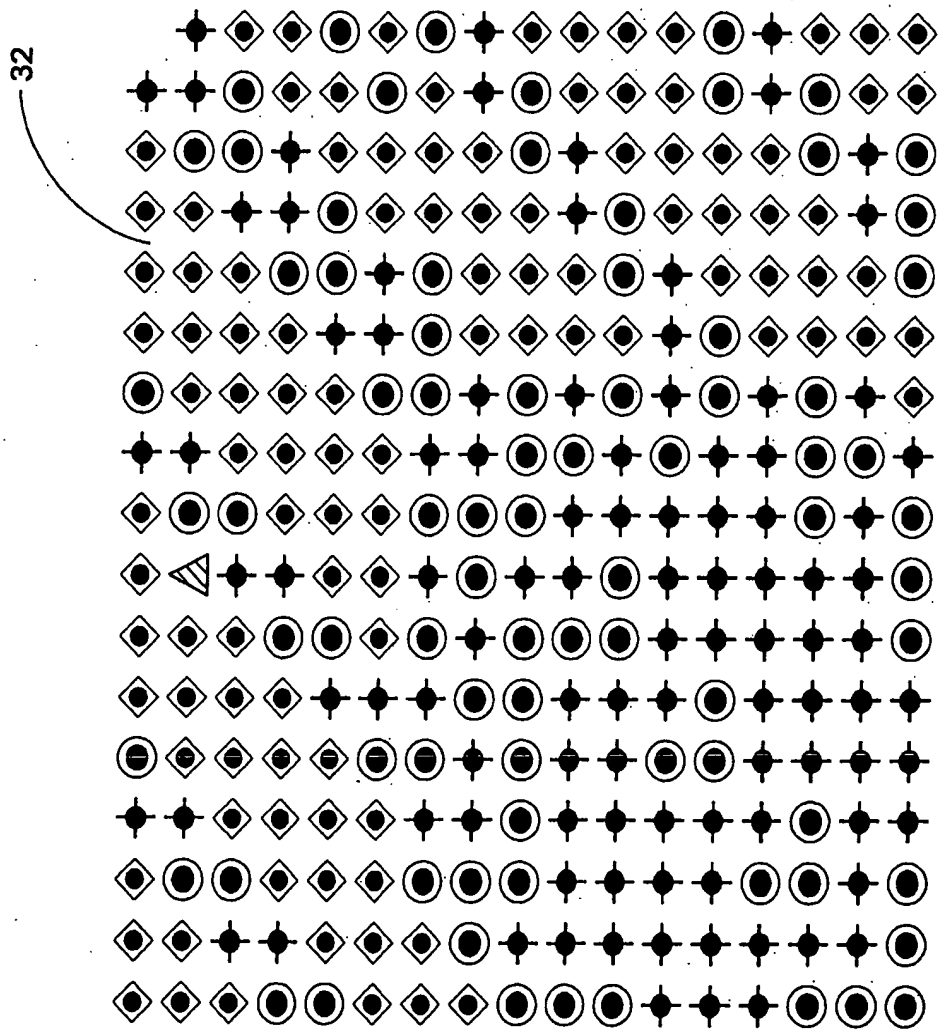


Figure 2

Figure 3



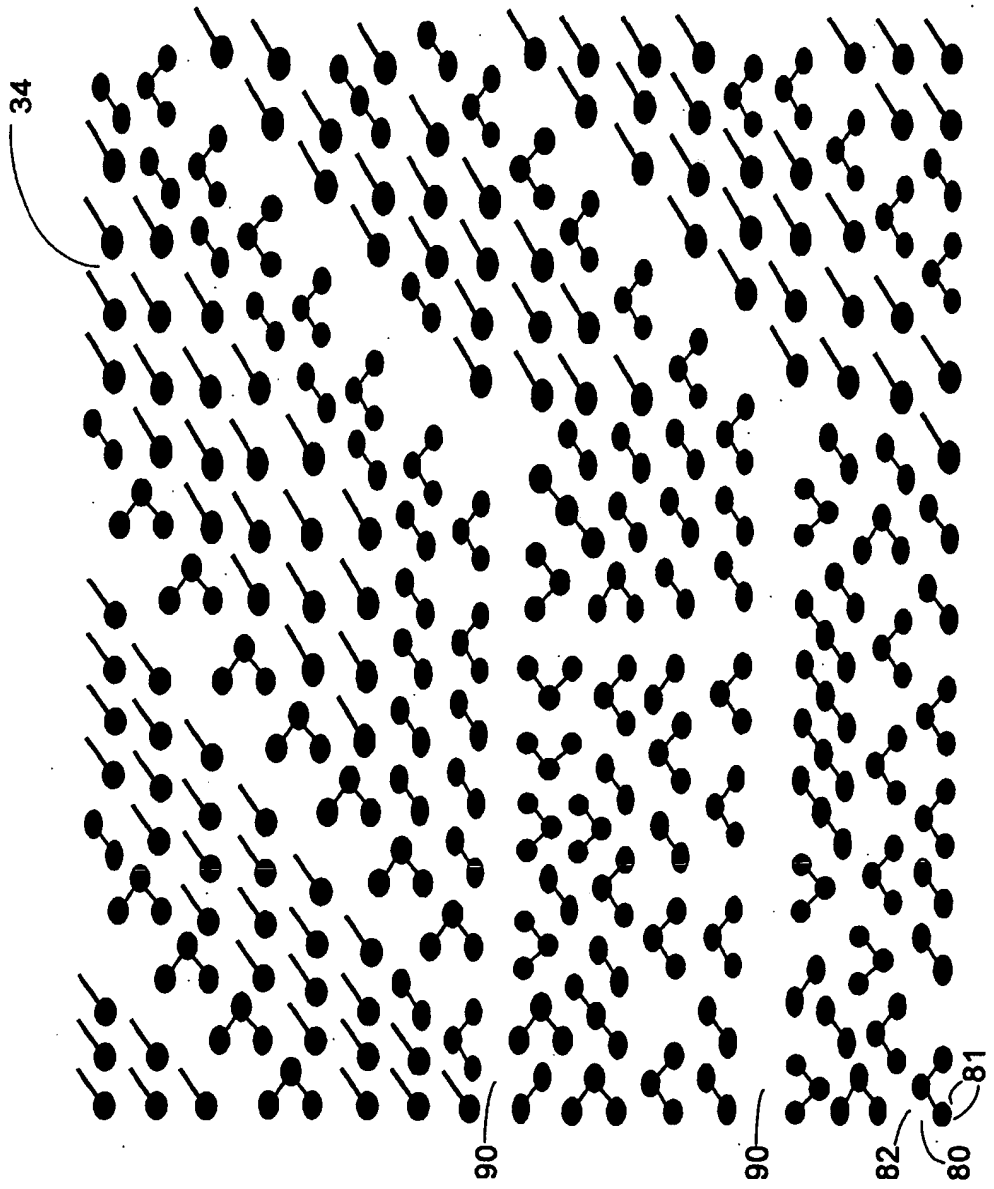


Figure 4A

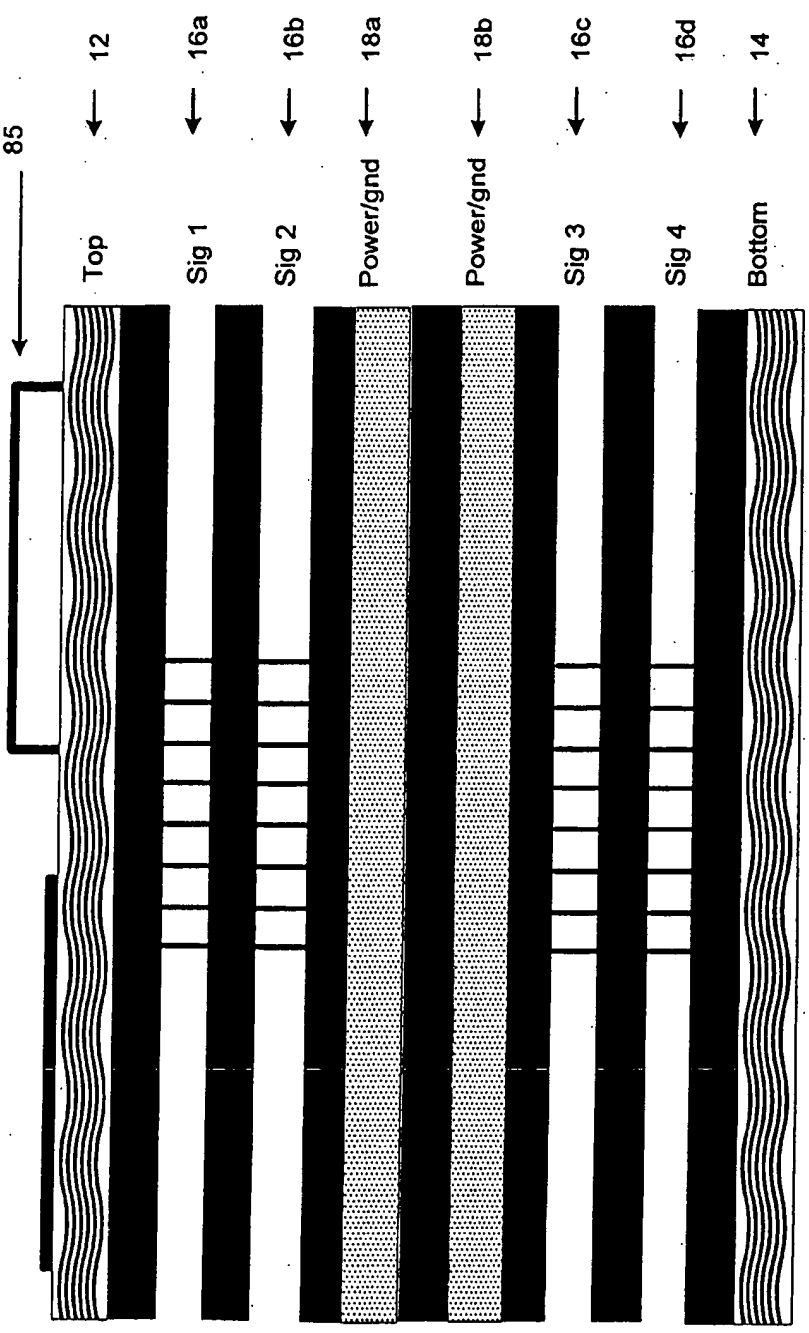

85
12
Top
16a
Sig 1
16b
Sig 2
18a
Power/gnd
18b
Power/gnd
16c
Sig 3
16d
Sig 4
14
Bottom

Figure 4B

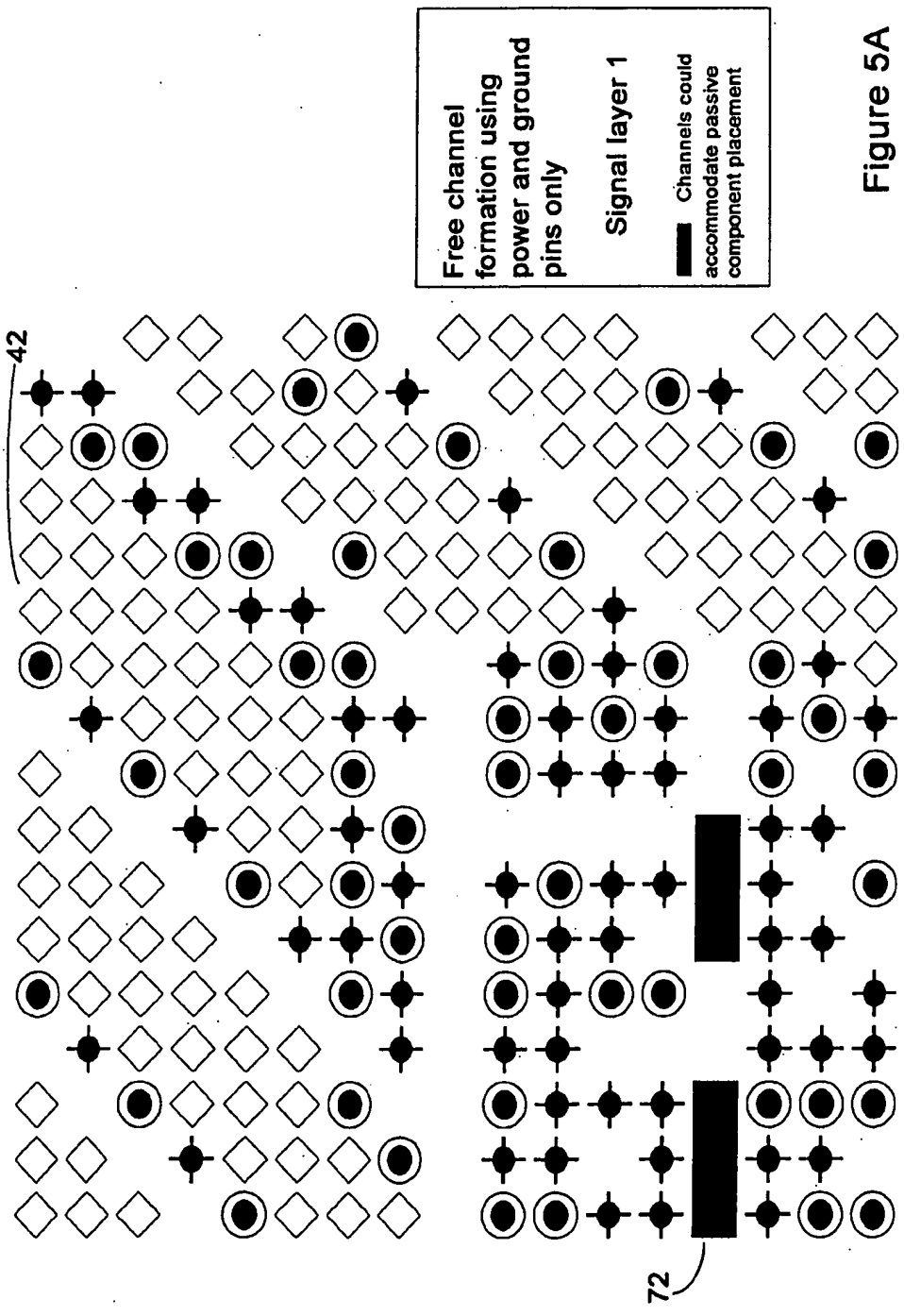

Free channel formation using power and ground pins only
Signal layer 1
Channels could accommodate passive component placement
42
72

Figure 5A

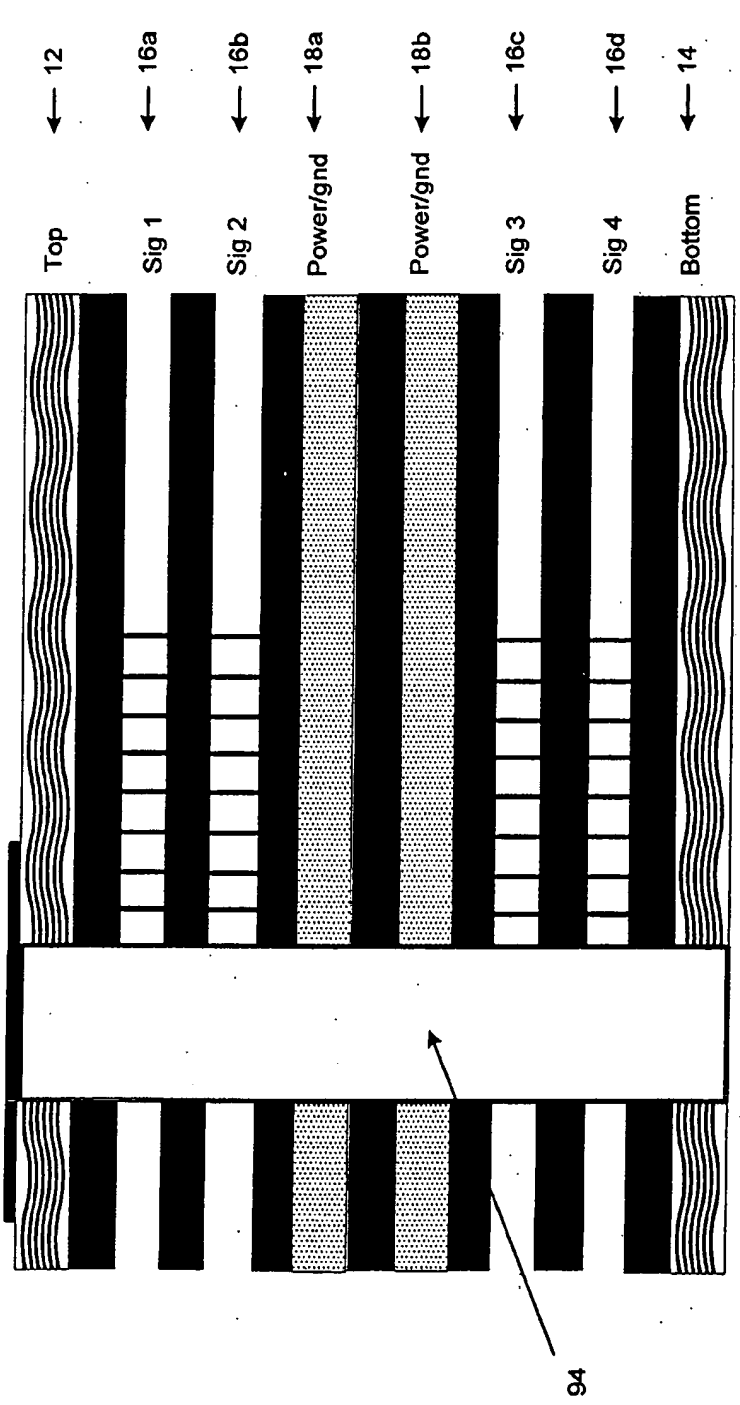

12
16a
16b
18a
18b
16c
16d
14
Top
Sig 1
Sig 2
Power/gnd
Power/gnd
Sig 3
Sig 4
Bottom
94

Figure 5B

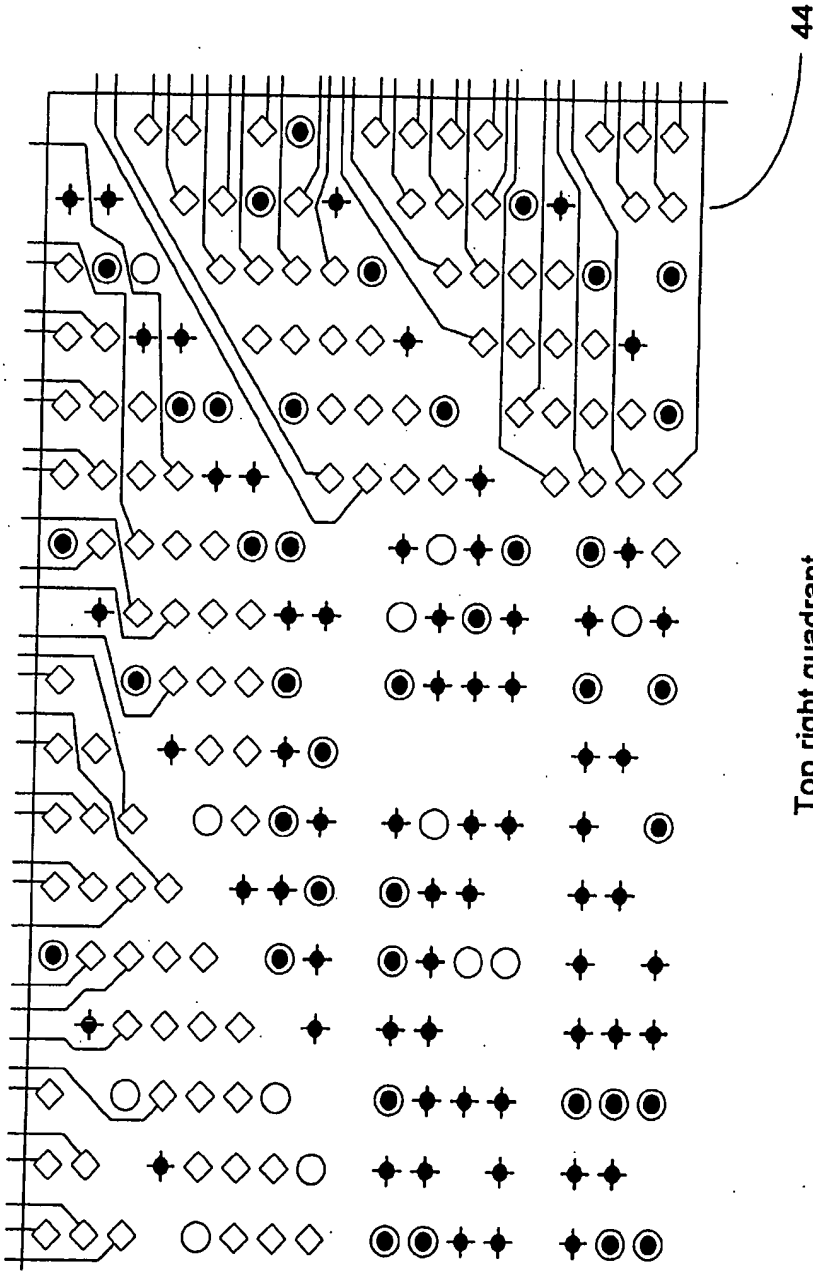


Figure 6A

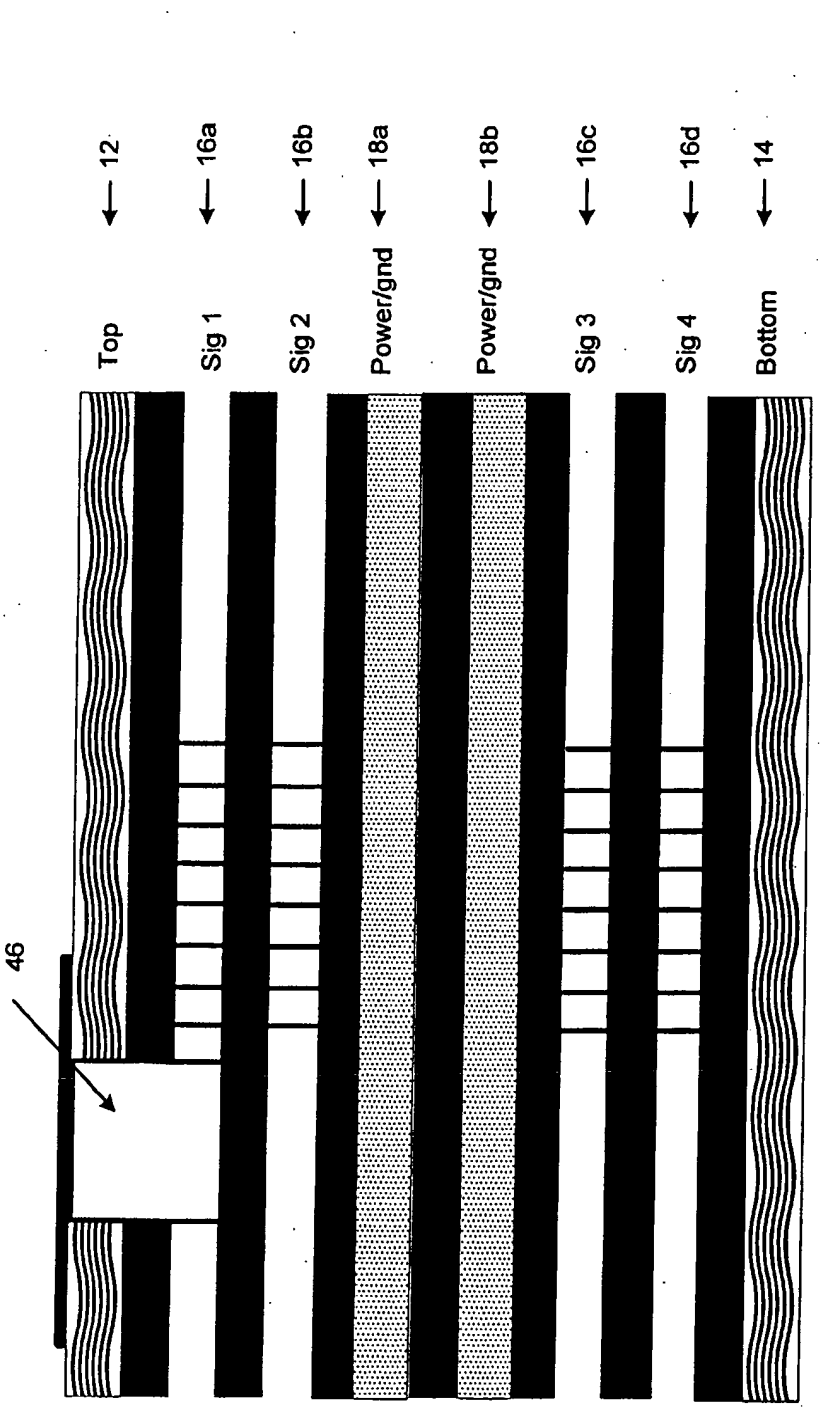

12
16a
16b
18a
18b
16c
16d
14
Top
Sig 1
Sig 2
Power/gnd
Power/gnd
Sig 3
Sig 4
Bottom
46

Figure 6B

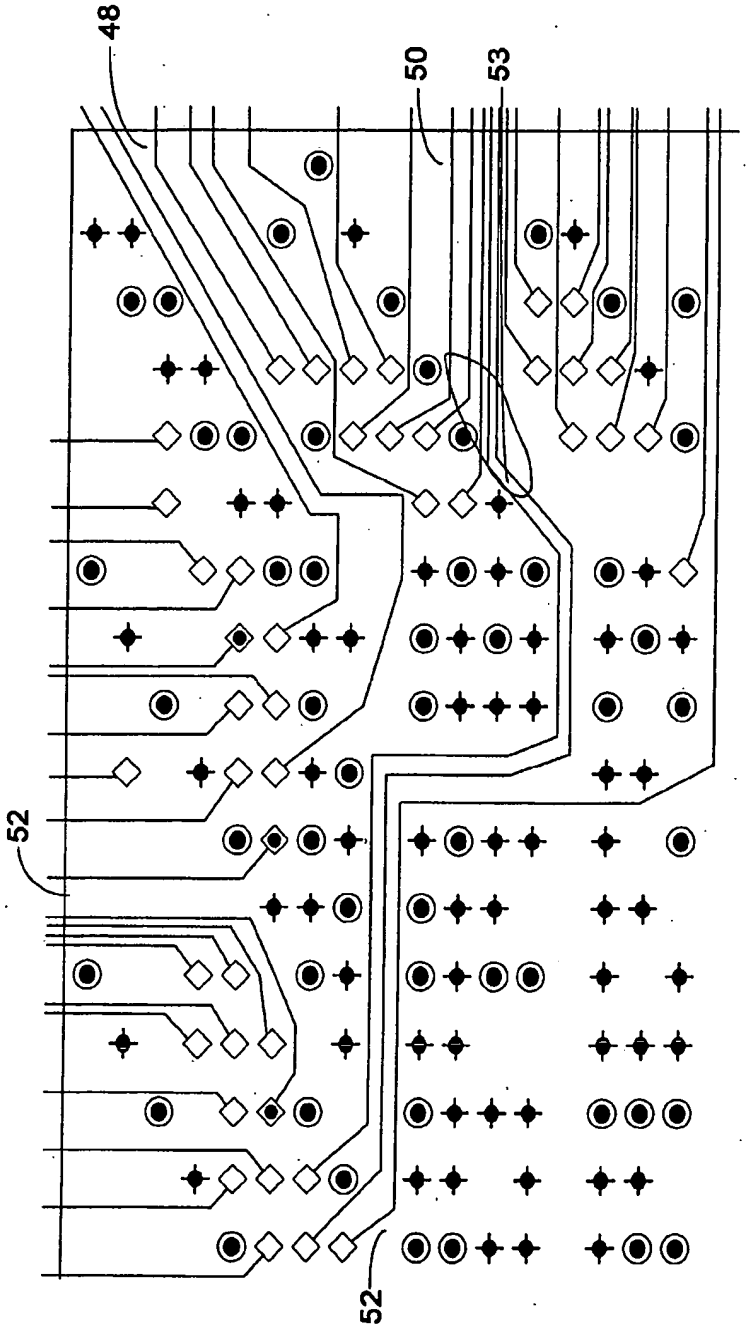


Figure 7A

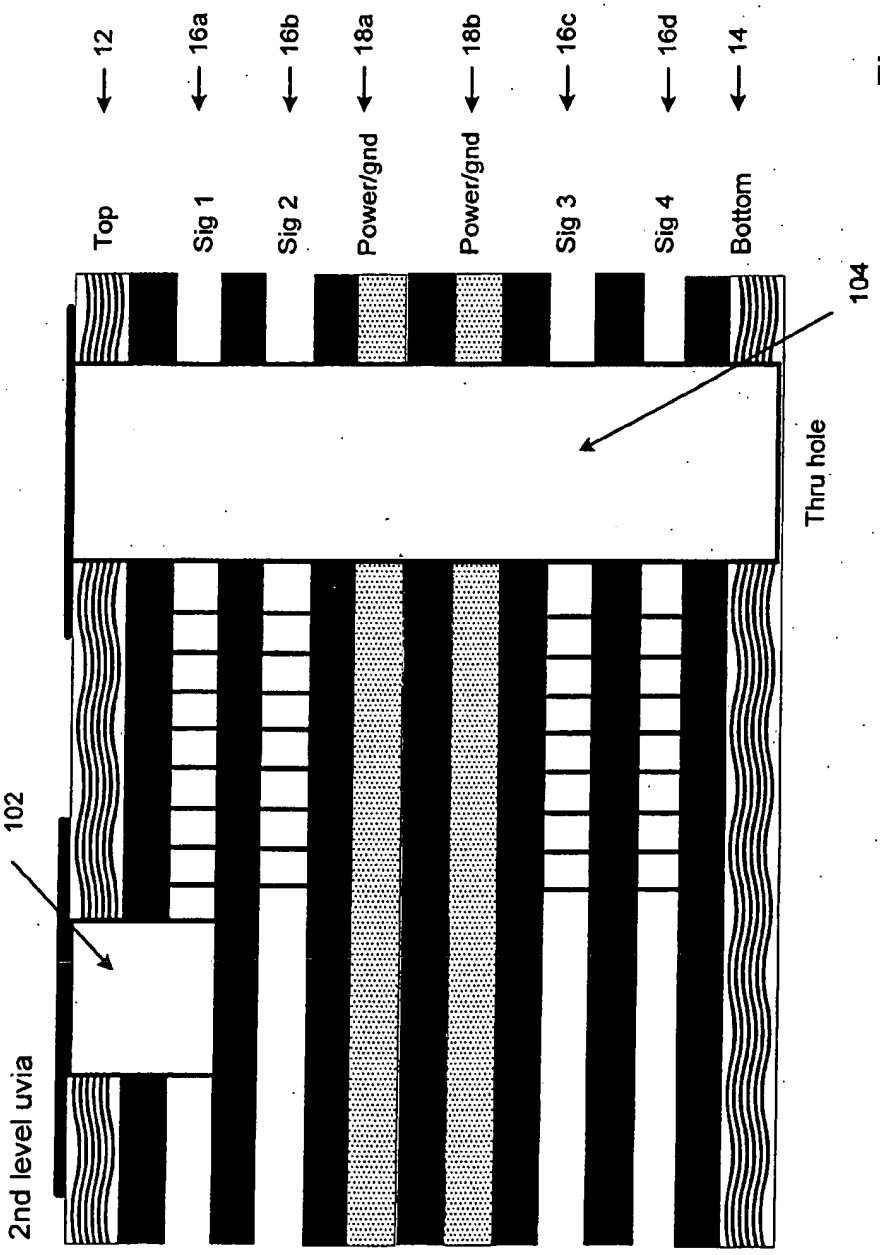

12
16a
16b
18a
18b
16c
16d
14
Top
Sig 1
Sig 2
Power/gnd
Power/gnd
Sig 3
Sig 4
Bottom
104
Thru hole
102
2nd level uvia

Figure 7B

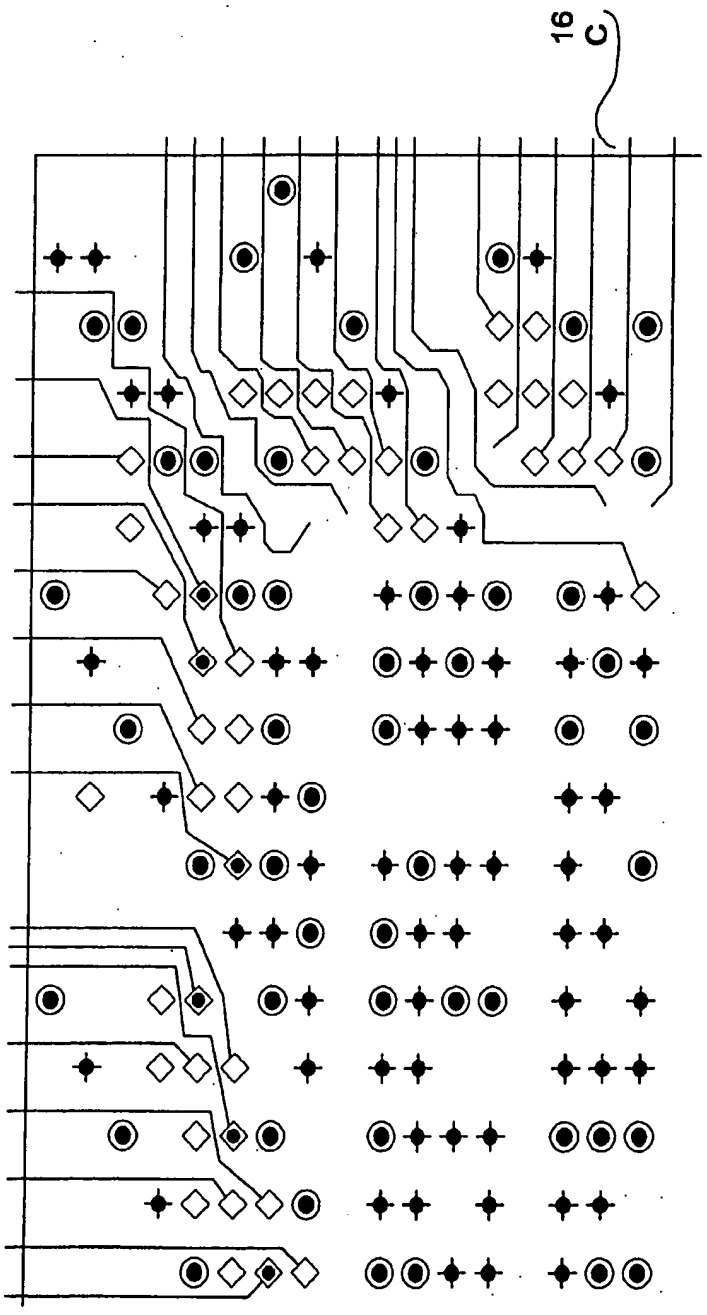


Figure 8

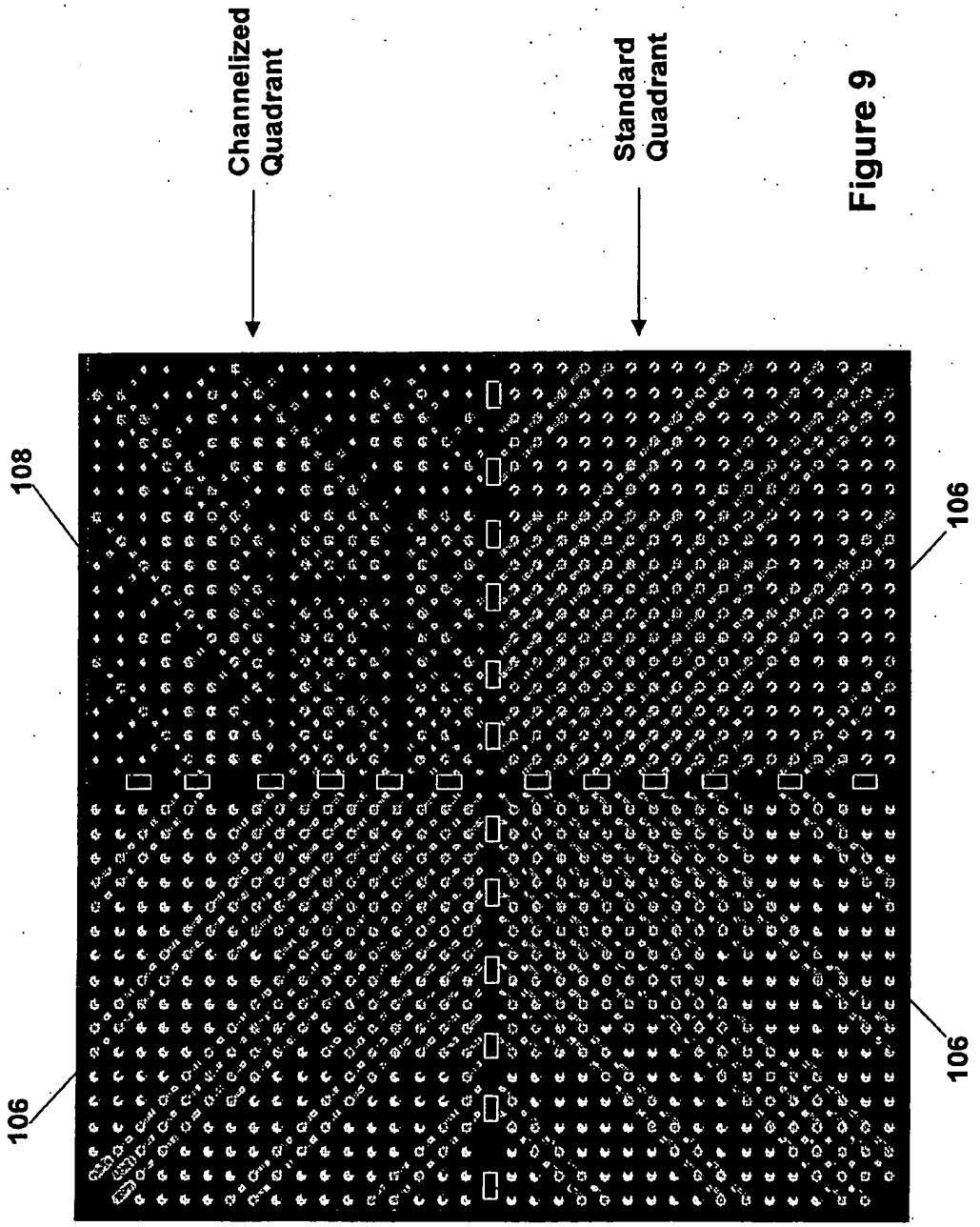


Figure 9

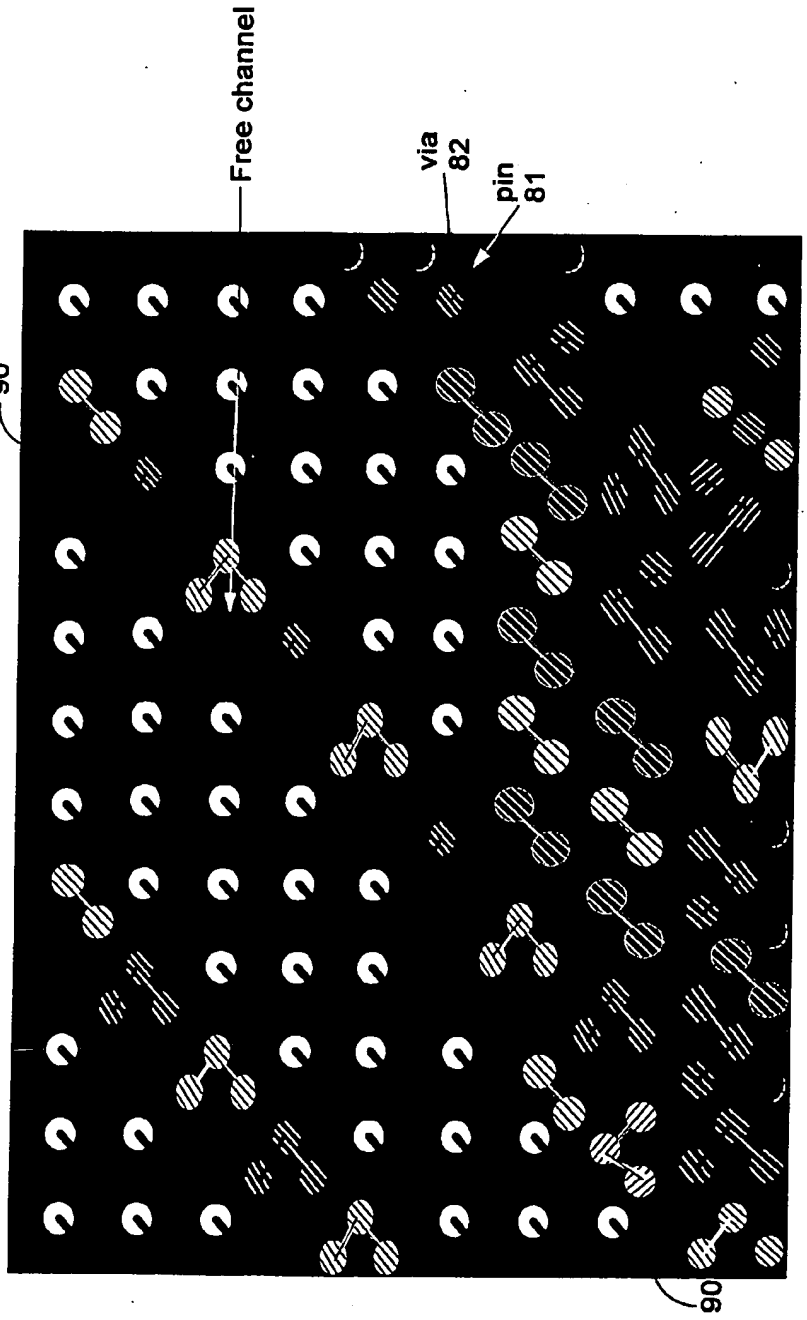
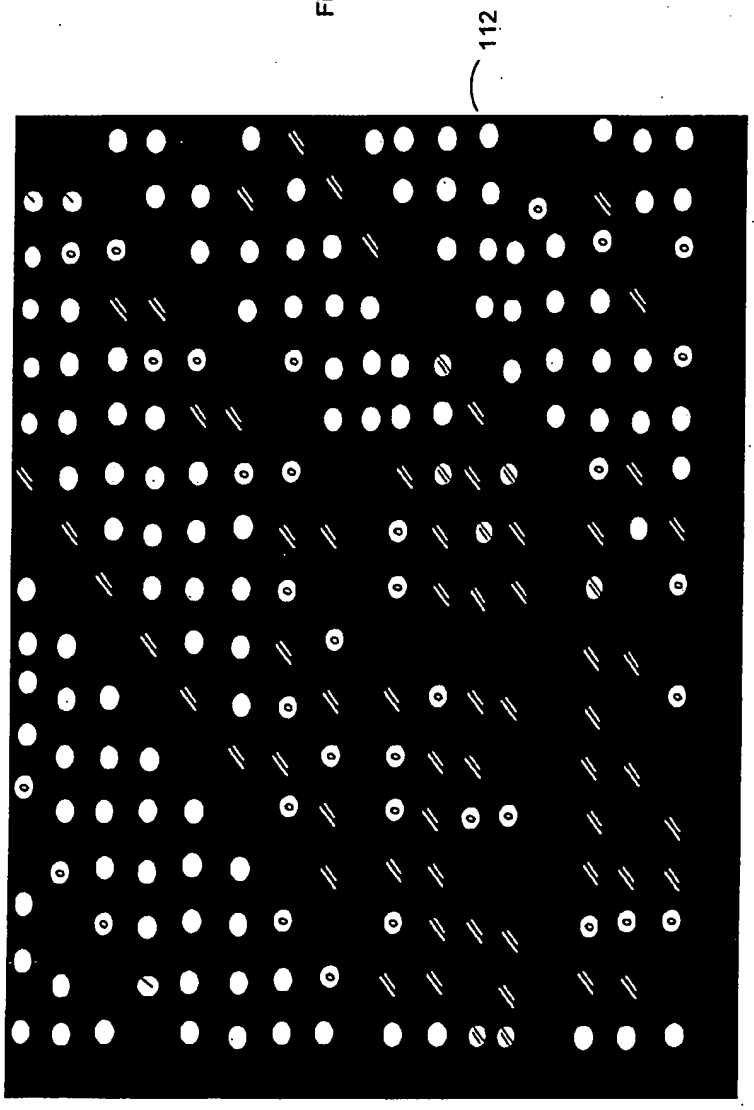


Figure 10

Figure 11



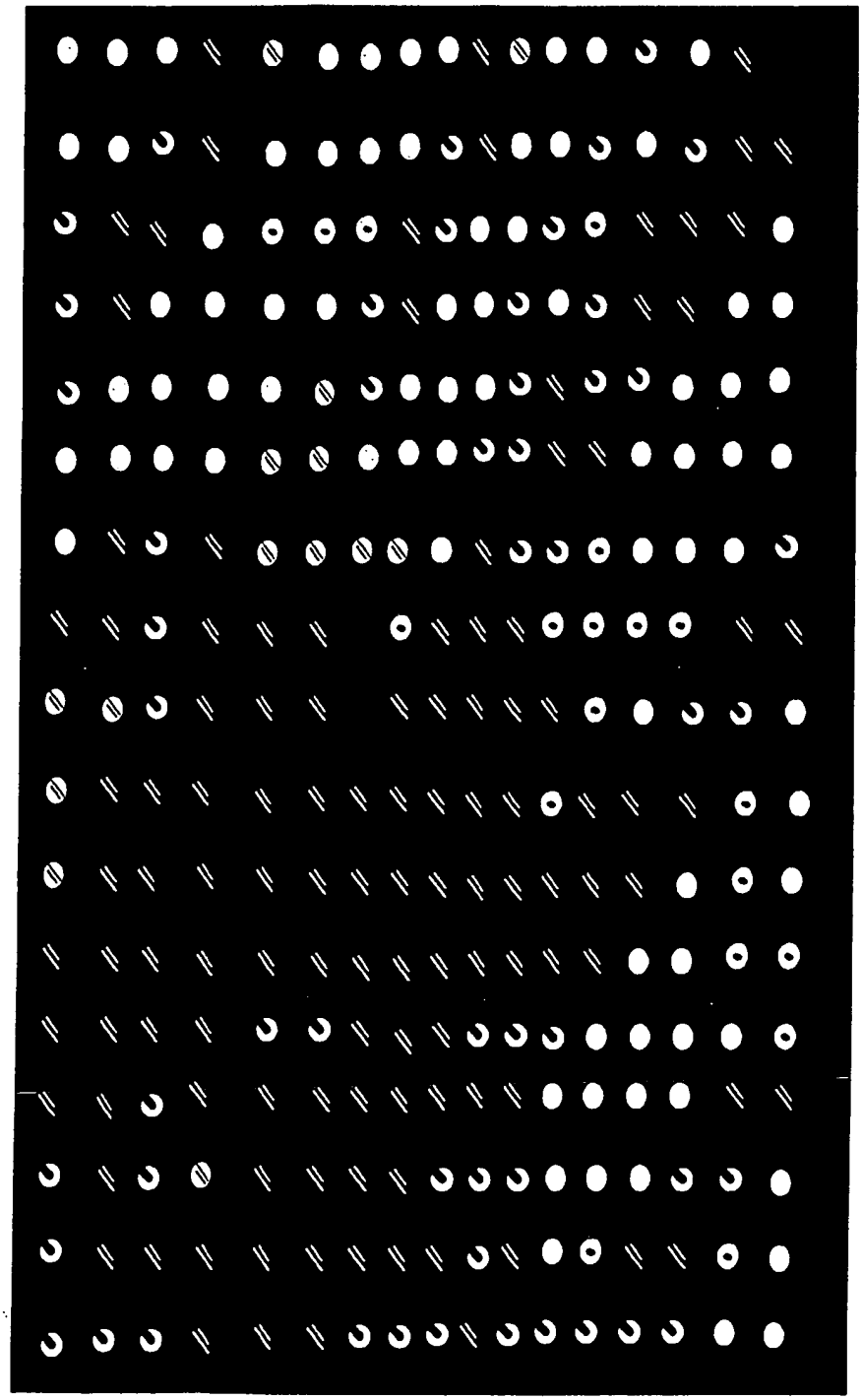


Figure 12